MOS TRANSISTOR WITH ELEVATED SOURCE AND DRAIN STRUCTURES AND METHOD OF FABRICATION THEREOF

ABSTRACT OF THE DISCLOSURE

A transistor and method of formation thereof includes source and drain extension regions in which the diffusion of dopants into the channel region is mitigated or eliminated. This is accomplished, in part, by elevating the source and drain extension regions into the epitaxial layer formed on the underlying substrate. In doing so, the effective channel length is increased, while limiting dopant diffusion into the channel region. In this manner, performance characteristics of the transistor can be accurately determined by controlling the respective geometries (i.e. depths and widths) of the source/drain extension regions, the source/drain regions, the channel width and an optional trench formed in the underlying substrate. In the various embodiments, the source/drain regions and the source/drain extension regions may extend partially, or fully, through the epitaxial layer, or even into the underlying semiconductor substrate.

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